This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

Claim 1 (canceled)

A memory, comprising:

a plurality of memory cells providing at least 256 meg of storage;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells;

a power supply;

a plurality of pads; and

not more than two layers of metal conductors providing interconnection between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads.

Claim 2 (canceled)

The memory of claim 1 wherein said memory is fabricated on a die approximately 24.7 mm by 15 mm.

Claim 3 (canceled)

The memory of claim 1 wherein said plurality of memory cells is arranged into a plurality of individual arrays, said individual arrays being organized into rows and columns to form a plurality of array blocks.

Claim 4 (canceled)

The memory of claim 3 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 5 (canceled)

The memory of claim 4 additionally comprising digitlines extending through each of said plurality of individual arrays and into said sense amplifiers, and I/O lines running between

adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 6 (canceled)

The memory of claim 5 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said IO lines, said plurality of peripheral devices including a plurality of multiplexors positioned at certain of said intersections of said I/O lines and said datelines for transferring signals on said I/O lines to said datalines.

Claim 7 (canceled)

The memory of claim 6 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 8 (canceled)

The memory of claim 7 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexors responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexors.

Claim 9 (canceled)

The memory of claim 8 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 10 (canceled)

The memory of claim 9 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 11 (canceled)

The memory of claim 3 wherein said metal conductors form a web around each array block and a grid within each array block.

Claim 12 (canceled)

The memory of claim 3 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

Claim 13 (canceled)

The memory of claim 12 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

Claim 14 (canceled)

The memory of claim 1 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

Claim 15 (canceled)

The memory of claim 1 wherein said pads are centrally located.

Claim 16 (canceled)

The memory of claim 15 wherein said power supply is positioned proximate to said pads.

Claim 17 (canceled)

The memory of claim 1 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

Claim 18 (canceled)

The memory of claim 17 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

Claim 19 (canceled)

A memory fabricated on a die, comprising:

a plurality of memory cells providing at least 256 meg of storage;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells;

a power supply;

a plurality of pads; and

layers of metal conductors for providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads, and wherein the die is approximately 24.7 mm by 15 mm.

Claim 20 (canceled)

The memory of claim 1 wherein said layers of metal do not exceed two.

Claim 21 (canceled)

The memory of claim 19 wherein said plurality of memory cells is arranged into a plurality of individual arrays, said individual arrays being organized into rows and columns to form a plurality of array blocks.

Claim 22 (canceled)

The memory of claim 21 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 23 (canceled)

The memory of claim 23 additionally comprising digitlines extending through each of said plurality of individual arrays and into said sense amplifiers, and I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 24 (canceled)

The memory of claim 23 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O

lines, said plurality of peripheral devices including a plurality of multiplexors, positioned at certain of said intersections of said I/O lines and said datalines for transferring signals on said I/O lines to said datalines.

Claim 25 (canceled)

The memory of claim 24 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a-plurality of-data output buffers -responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 26 (canceled)

The memory of claim 25 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 27 (canceled)

The memory of claim 26 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 28 (canceled)

The memory of claim 27 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 29 (canceled)

The memory of claim 21 wherein said metal conductors form a web around each array block and a grid within each array block.

Claim 30 (canceled)

The memory of claim 21 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

Claim 31 (canceled)

The memory of claim 30 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

Claim 32 (canceled)

The memory such that of claim 19 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

Claim 33 (canceled)

The memory of claim 19 wherein said pads are centrally located.

Claim 34 (canceled)

The memory of claim 33 wherein said power supply is positioned proximate to said pads.

Claim 35 (canceled)

The memory of claim 19 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

Claim 36 (canceled)

The memory of claim 35 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

Claim 37 (canceled)

A memory, comprising:

a plurality of memory cells providing at least 256 meg of storage, said memory calls being fabricated at a density of 791,350 bits per square mil;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells;

a power supply;

a plurality of pads; and

layers of metal conductors for providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads.

Claim 38 (canceled)

The memory of claim 37 wherein said layers of metal do not exceed two.

Claim 39 (canceled)

The memory of claim 37 wherein said memory is fabricated on a die approximately 24.7 mm by 15 mm.

Claim 40 (canceled)

The memory of claim 37 wherein said plurality of memory cells is arranged into a plurality of individual arrays, said individual arrays being organized into rows and columns to form a plurality of array blocks.

Claim 41 (canceled)

The memory of claim 40 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 42 (canceled)

The memory of claim 41 additionally comprising digitlines extending through each of said plurality of individual arrays and into said sense amplifiers, and I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 43 (canceled)

The memory of claim 42 additionally comprising datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O

lines, said plurality of peripheral devices including a plurality of multiplexers, positioned at certain of said intersections of said I/O lines and said data lines for transferring signals on said I/O lines to said data lines.

Claim 44 (canceled)

The memory of claim 43 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 45 (canceled)

The memory of claim 44 wherein said plurality of peripheral devices includes a plurality of data in buffers response to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 46 (canceled)

The memory of claim 45 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 47 (canceled)

The dynamic random access memory of claim 46 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 48 (canceled)

The memory of claim 40 wherein said metal conductors form a web around each array block and a grid within each array block.

Claim 49 (canceled)

The memory of claim 40 additionally comprising switches for disconnecting each of said plurality of array blocks from said power supply.

Claim 50 (canceled)

The memory of claim 49 wherein said power supply has a modular design such that certain modules can be shut down in response to the number of array blocks connected to said power supply.

Claim 51 (canceled)

The memory of claim 37 wherein said power supply has a modular design such that certain modules can be shut down in response to a refresh mode of operation.

Claim 52 (canceled)

The memory of claim 37 wherein said pads are centrally located.

Claim 53 (canceled)

The memory of claim 52 wherein said power supply is positioned proximate to said pads.

Claim 54 (canceled)

The memory of claim 37 wherein said power supply includes a voltage regulator for producing an array voltage, voltage pumps for producing boosted voltages, and a voltage generator for producing a bias voltage for use by said random access memory.

Claim 55 (canceled)

The memory of claim 54 additionally comprising a sequence circuit for controlling the sequence in which said voltage regulator, voltage pumps, and voltage generator are powered up.

Claim 56 (canceled)

A die carrying a 256 meg memory device, said die having not more than two layers of metal conductors.

Claim 57 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of pads located centrally with respect to said array blocks;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies located proximate said plurality of pads for generating a plurality of supply voltages; and

a power distribution bus for delivering said plurality of supply voltages to said individual arrays and said plurality of peripheral devices.

Claim 58 (canceled)

A power distribution bus for a memory device constructed of memory blocks organized into an array, said bus comprised of a first plurality of conductors for carrying the voltages used by the array and forming a web surrounding each of the blocks of the array, and a second plurality of conductors extending from said web into each of the memory blocks to form a grid within each of the memory blocks.

Claim 59 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and wherein said power amplifiers are organized into a plurality of groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power, and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

Claim 60 (canceled)

A voltage regulator for a dynamic random access memory, said voltage regulator comprising:

a voltage reference circuit for producing a reference voltage;

a plurality of power amplifiers for developing a supply voltage for supplying power to the dynamic random access memory, said power amplifiers being responsive to said reference voltage and having a gain greater than one; and

a control circuit for producing control signals for controlling said plurality of power amplifiers.

Claim 61 (canceled)

A dynamic random access memory, comprising:

an array of memory cells configured in separately controllable array blocks;

a plurality of peripheral devices responsive to external signals for writing data into said array blocks and for reading data out of said array blocks;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and at least one of-said power amplifiers being-associated with each of said array blocks;

a plurality of power distribution switches; and

a power distribution bus for delivering said plurality of supply voltages to said array blocks through said plurality of switches and to said plurality of peripheral devices, and wherein

said plurality of peripheral devices includes logic for controlling each of said plurality of switches and for controlling the state of each of said power amplifiers.

Claim 62 (canceled)

A voltage regulator for a dynamic random access memory having an array divided into array blocks, said voltage regulator comprising:

a voltage reference circuit for producing a reference voltage;

multiple power amplifiers for developing a supply voltage, said power amplifiers arranged such that certain of said power amplifiers supply power to certain of the array blocks; and

control circuitry for disabling a power amplifier when the array block associated therewith is disabled.

Claim 63 (canceled)

A power supply for a dynamic random access memory having a plurality of array blocks and a plurality of pads located centrally of the array blocks, said power supply comprising:

a plurality of voltage supplies located proximate to the plurality of pads for producing supply voltages for the plurality of array blocks.

Claim 64 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage pump comprised of a plurality of voltage pump circuits and

wherein said voltage pump circuits are organized into a plurality of supply groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

Claim 65 (canceled)

A voltage pump for an integrated circuit, comprising:

a plurality of voltage pump circuits operable in response to a clock signal input thereto, said plurality of voltage pump circuits being divided into a plurality of groups for operation in response to an enable signal produced by the integrated circuit in one of separate or concurrent operating modes to achieve predetermined levels of power output;

an oscillator circuit for producing said clock signal; and

a regulator circuit for producing first signals for controlling said oscillator circuit.

Claim 66 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices, one of said plurality of voltage supplies including a voltage generator producing an output voltage;

a voltage detection circuit responsive to said output voltage for producing an overvoltage signal and an undervoltage signal indicative of whether the output voltage is within a first predetermined range; and

a logic circuit responsive to said overvoltage and said undervoltage signals for providing an indication-of-the stability-of-the -voltage generator.

Claim 67 (canceled)

A stability sensor for a voltage generator which utilizes pullup and pulldown currents for regulation purposes, said sensor comprising:

a current source responsive to one of the pullup and pulldown currents for producing a source current indicative of the current;

a resistor for generating a voltage in response to the source current; and

an overcurrent circuit responsive to said voltage for producing a signal indicative of an excessive amount of one of the pullup and pulldown current.

Claim 68 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

a powerup sequence circuit for controlling the powering up of certain of the plurality of voltage supplies in response to the condition of previously powered up voltage supplies.

Claim 69 (canceled)

A powerup circuit for an integrated circuit having a voltage supply responsive to a voltage external to the integrated circuit and generating a feedback signal, said powerup circuit comprising:

a first circuit portion responsive to the external voltage for producing a first output signal indicative of whether the external voltage is above a predetermined value; and

a second circuit portion responsive to said first output signal and the feedback signal for producing a first enable signal to enable the voltage supply.

Claim 70 (canceled)

A dynamic random access memory, comprising:

an array of memory cells, each comprised of two storage elements;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

test mode logic for determining whether the memory is in a test mode, and wherein said plurality of peripheral devices includes a latch circuit responsive to a first external signal when the memory is in the test mode, for latching data stored in a first group of memory elements, and a write enable circuit responsive to a second external signal when said memory is in the test mode, for enabling the latched data to be written to a second group of memory elements.

Claim 71 (canceled)

A method of testing a plurality of memory elements organized in a plurality of rows, comprising the steps of:

writing test data into a first row of memory elements;

latching the test data from the first row of memory elements in response to a first external signal;

writing the latched test data into a first group of memory elements in response to a second external signal;

reading the test data from the second group of memory elements; and

comparing the test data read from the second group of memory elements with the test data written to the first row of memory elements.

Claim 72 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing information into said memory cells and for reading information out of said memory cells, said plurality of peripheral devices including a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks; and

a plurality of voltage supplies for generating a plurality of supply voltages for use by said array blocks and said plurality of peripheral devices, and wherein

said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said IO lines, and wherein

said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said 110 lines to said datalines.

Claim 73 (canceled)

A data path for a dynamic random access memory having a plurality of data cells organized into rows and columns to form a plurality of individual arrays, the plurality of individual arrays organized into rows and columns to form a plurality of array blocks, with the array blocks organized into a plurality of quadrants, said data path comprising:

a plurality of sense amplifiers positioned between adjacent rows of individual arrays;

a plurality of digitlines extending through each individual array and into said sense amplifiers;

a plurality of I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines;

a plurality of datalines running between adjacent columns of individual arrays to form intersections with said I/O lines;

a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said VO lines to said datalines;

a plurality of I/O blocks each responsive to said datalines from one of said plurality of array quadrants;

a plurality of data read multiplexers responsive to said array I/O blocks;

a plurality of data output buffers responsive to said plurality data read multiplexers; a plurality of data pad drivers responsive to said plurality of data output buffers for

making data read from the cells available at a plurality of pads;

a plurality of data in buffers responsive to data available at the plurality of pads; and

a plurality of data write multiplexers responsive to said plurality of data in buffers, and

wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 74 (canceled)

An output buffer, comprising:

a plurality of output drive transistors connected in series between a first voltage supply and ground;

an output terminal responsive to said series connected transistors;

a latch for receiving data to be output to said output terminal;

a logic circuit responsive to said latch for controlling said output drive transistors to drive

a voltage at said output terminal to one of a high and low potential representing a logic state of the data to be output;

a boot capacitor for supplying additional voltage to certain of said drive transistors;

a holding transistor responsive to said logic circuit for connecting said boot capacitor to a second supply voltage; and

a self-timed circuit path connected across said holding transistor and said boot capacitor.

Claim 75 (canceled)

A dynamic random access memory, comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into and reading data out of said array of

memory cells, said peripheral devices including a plurality of programmable multiplexer cells;

a power supply;

a plurality of pads; and

layers of conductors providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said power supply, and said plurality of pads.

Claim 76 (canceled)

A programmable multiplexer cell for use in a memory device, comprising:

a plurality of input lines;

a plurality of output lines;

a plurality of programmable switches connecting said plurality of input lines to said plurality of output lines through said multiplexer.

Claim 77 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays having digitlines extending there through, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing data into and for reading data out of said memory cells with said digitlines;

a power supply for generating a plurality of supply voltages, said power supply voltages including a plurality of generators for producing a bias voltage for biasing said digitlines, said number of generators being equal to said number of array blocks; and

a power distribution bus for delivering said plurality of supply voltages to said plurality of array blocks and said peripheral devices.

Claim 78 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays having digitlines extending therethrough;

a plurality of peripheral devices for writing data into and for reading data out of said memory cells with said digitlines, said peripheral devices including a plurality of sense amplifiers

for sensing the signals on said digitlines, said sense amplifiers being controlled by control signals having a greater magnitude than the magnitude of the data signals to be written to said memory cells;

a power supply for generating a plurality of supply voltages; and

a power distribution bus for delivering said plurality of supply voltages to said individual arrays and said peripheral devices.

Claim 79 (canceled)

A sense amplifier, comprising:

a digitline for connecting an array to I/O lines;

an equalization switch adjacent the array for equilibrating said digitline;

an n-sense amplifier connected across said digitline;

a p-sense amplifier connected across said digitline;

an isolation switch connected between said n-sense and said p-sense amplifier and said equalization switch for isolating said n-sense and p-sense amplifier from the array; and a connection switch for connecting said digitline to the I/O line.

Claim 80 (canceled)

A dynamic random access memory, comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of peripheral devices for writing information into and reading information out of said plurality of memory cells, said plurality of peripheral devices including a plurality of sense amplifiers;

logic for producing a redundant signal for controlling said plurality of peripheral devices; a power supply;

a plurality of pads; and

not more than a first layer and a second layer of metal conductors providing interconnections between said plurality of memory cells, said plurality of peripheral devices, said logic, said power supply, and said plurality of pads, said redundant signal being routed through said sense amplifiers in said second layer of metal.

Claim 81 (canceled)

The memory of claim 57 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 82 (canceled)

The memory of claim 81 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 83 (canceled)

The memory of claim 82 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 84 (canceled)

The memory of claim 83 wherein said multiplexers are positioned at every second individual array.

Claim 85 (canceled)

The memory of claim 57 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 86 (canceled)

The memory of claim 85 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 87 (canceled)

The memory of claim 85 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 88 (canceled)

The memory of claim 87 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 89 (canceled)

The memory of claim 57 wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 90 (canceled)

The memory of claim 89 wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 91 (canceled)

The memory of claim 57 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 92 (canceled)

The memory of claim 91 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 93 (canceled)

The memory of claim 91 wherein said plurality of power amplifiers are divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

Claim 94 (canceled)

The memory of claim 57 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate or concurrent operation to achieve predetermined levels of output power.

Claim 95 (canceled)

The memory of claim 94 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 96 (canceled)

The memory of claim 57 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

Claim 97 (canceled)

The memory of claim 57 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 98 (canceled)

The memory of claim 57 wherein said memory provides at least 256 meg of storage.

Claim 99 (canceled)

The memory of claim 98 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace

defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 100 (canceled)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

a plurality of individual arrays of memory cells, said individual arrays organized into rows and columns to form a plurality of array blocks;

a plurality of pads located centrally with respect to said array blocks;

a plurality of peripheral devices for transferring data between said memory cells and said plurality of pads;

a plurality of voltage supplies located proximate said plurality of pads for generating a plurality of supply voltages; and

a power distribution bus for delivering said plurality of supply voltages to said individual arrays and said plurality of peripheral devices.

Claim 101 (canceled)

The system claim 100 wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 102 (canceled)

The system of claim 101 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 103 (canceled)

The system of claim 102 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 104 (canceled)

The system of claim 103 wherein said multiplexers are positioned at every second individual array.

Claim 105 (canceled)

The system of claim 100 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers for making the read data available at said plurality of pads.

Claim 106 (canceled)

The system of claim 105 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to data available at said plurality of pads and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 107 (canceled)

The system of claim 105 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 108 (canceled)

The system of claim 107 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 109 (canceled)

The system of claim 100 wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 110 (canceled)

The system of claim 109 wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 111 (canceled)

The system of claim 100 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 112 (canceled)

The system of claim 111 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 113 (canceled)

The system of claim 111 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate or concurrent operation to achieve a predetermined level of output power.

Claim 114 (canceled)

The system of claim 100 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate or concurrent operation to achieve predetermined levels of output power.

Claim 115 (canceled)

The system of claim 114 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 116 (canceled)

The system of claim 100 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

Claim 117 (canceled)

The system of claim 100 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 118 (canceled)

The system of claim 100 wherein said memory provides at least 256 meg of storage.

Claim 119 (canceled)

The system of claim 118 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 120 (canceled)

The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying an array voltage.

Claim 121 (canceled)

The power distribution bus of claim 120 additionally comprising a plurality of switches each controlling the distribution of the array voltage to one of the array blocks.

Claim 122 (canceled)

The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a boosted array voltage.

Claim 123 (canceled)

The power distribution bus of claim 122 additionally comprising a plurality of switches each controlling the distribution of the boosted array voltage to one of the array blocks.

Claim 124 (canceled)

The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a digitline bias voltage.

Claim 125 (canceled)

The power distribution bus of claim 124 additionally comprising a plurality of switches each controlling the distribution of the digitline bias voltage to one of the array blocks.

Claim 126 (canceled)

The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a ground voltage.

Claim 127 (canceled)

The power distribution bus of claim 126 additionally comprising a plurality of switches each controlling the distribution of the ground voltage to one of the array blocks.

Claim 128 (canceled)

The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a back bias voltage.

Claim 129 (canceled)

The power distribution bus of claim 128 additionally comprising a plurality of switches each controlling the distribution of the back bias voltage to one of the array blocks.

Claim 130 (canceled)

The power distribution bus of claim 58 wherein certain of said first and second pluralities of conductors are for carrying a cell plate voltage.

Claim 131 (canceled)

The power distribution bus of claim 130 additionally comprising a plurality of switches each controlling the distribution of the cell plate voltage to one of the array blocks.

Claim 132 (canceled)

The power distribution bus of claim 58 wherein certain of said first plurality of conductors are for carrying a peripheral voltage.

Claim 133 (canceled)

The power distribution bus of claim 132 additionally comprising a plurality of switches each controlling the distribution of the peripheral voltage to one of the array blocks.

Claim 134 (canceled)

The power distribution bus of claim 58 wherein said first plurality of conductors extend from an area located centrally with respect to the memory blocks.

Claim 135 (canceled)

The power distribution bus of claim 58 additionally comprising a third plurality of conductors running parallel to a plurality of input/output pads for receiving external power from the pads and for supplying the external power to a plurality of voltage supplies located proximate to the pads.

Claim 136 (canceled)

A system for generating and distributing power to a memory device constructed of memory blocks and organized into an array, said system comprising:

a plurality of voltage supplies located centrally with respect to the memory blocks of the array and for producing a plurality of operating voltages; and

a first plurality of conductors forming a web surrounding each of the blocks of the array, one of said conductors being responsive to ground potential, said other conductors being responsive to the plurality of operating voltages.

Claim 137 (canceled)

The system of claim 136 wherein one of said plurality of voltage supplies includes a voltage regulator for producing an array voltage and a peripheral voltage.

Claim 138 (canceled)

The system of claim 136 wherein one of said plurality of voltage supplies includes a voltage pump for producing a back bias voltage.

Claim 139 (canceled)

The system of claim 136 wherein one of said plurality of voltage supplies includes a generator for producing a cellplate and digitline bias voltage.

Claim 140 (canceled)

The system of claim 136 wherein one of said plurality of power supplies includes a voltage pump for producing a boosted array voltage.

Claim 141 (canceled)

The system of claim 136 additionally comprising a second plurality of conductors extending from said web into each of the memory blocks to form a grid within each of the memory blocks.

Claim 142 (canceled)

The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying an array voltage.

Claim 143 (canceled)

The system of claim 142 additionally comprising a plurality of switches each controlling the distribution of the array voltage to one of the memory blocks.

Claim 144 (canceled)

The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying a boosted array voltage.

Claim 145 (canceled)

The system of claim 144 additionally comprising a plurality of switches each controlling the distribution of the boosted array voltage to one of the memory blocks.

Claim 146 (canceled)

The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying a digitline bias voltage.

Claim 147 (canceled)

The system of claim 146 additionally comprising a plurality of switches each controlling the distribution of the digitline bias voltage to one of the memory blocks.

Claim 148 (canceled)

The system claim 141 wherein certain of said first and second pluralities of conductors are for carrying a ground voltage.

Claim 149 (canceled)

The system of claim 148 additionally comprising a plurality of switches each controlling the distribution of the ground voltage to one of the memory blocks.

Claim 150 (canceled)

The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying a back bias voltage.

Claim 151 (canceled)

The system of claim 150 additionally comprising a plurality of switches each controlling the distribution of the back bias voltage to one of the memory blocks.

Claim 152 (canceled)

The system of claim 141 wherein certain of said first and second pluralities of conductors are for carrying a cell plate voltage.

Claim 153 (canceled)

The system of claim 152 additionally comprising a plurality of switches each controlling the distribution of the cell plate voltage to one of the memory blocks.

Claim 154 (canceled)

The system of claim 141 additionally comprising a plurality of input/output pads for receiving external power and positioned proximate to said plurality of voltage supplies.

Claim 155 (canceled)

The system of claim 154 additionally comprising a third plurality of conductors for connecting certain of said plurality of input/output pads to said plurality of voltage supplies.

Claim 156 (canceled)

The system of claim 155 wherein certain of said third plurality of conductors are for carrying an external voltage.

Claim 157 (canceled)

The system of claim 155 wherein certain of said third plurality of conductors are for carrying a pad driver external voltage.

Claim 158 (canceled)

The system of claim 155 wherein certain of said third plurality of conductors are for carrying a pad driver ground potential.

Claim 159 (canceled)

A method of generating and distributing voltages to a dynamic random access memory device having a plurality of memory blocks arranged in an array and a plurality of pads located centrally of said array of memory blocks, said method comprising the steps of:

generating a plurality of voltages with a plurality of voltage supplies positioned proximate to the plurality of pads;

distributing said plurality of voltages through a web surrounding each of the blocks of the array, and

distributing certain of said plurality of voltages into each of the memory blocks through a second plurality of conductors extending from said web into each of the memory blocks.

Claim 160 (canceled)

The method of claim 159 additionally comprising the step of distributing to the voltage supplies through a third plurality of conductors certain voltages available at the pads.

Claim 161 (canceled)

The method of claim 159 additionally comprising the step of controlling the distribution of said plurality of voltages with a plurality of switches.

Claim 162 (canceled)

The memory of claim 59 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein one of said power amplifiers is associated with each of said plurality of array blocks.

Claim 163 (canceled)

The memory of claim 162 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 164 (canceled)

The memory of claim 59 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate or concurrent operation to achieve predetermined levels of output power.

Claim 165 (canceled)

The memory of claim 164 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 166 (canceled)

The memory of claim 59 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 167 (canceled)

The memory of claim 59 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 168 (canceled)

The memory of claim 59 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 169 (canceled)

The memory of claim 168 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 170 (canceled)

The memory of claim 169 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with

said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 171 (canceled)

The memory of claim 170 wherein said multiplexers are positioned at every second individual array.

Claim 172 (canceled)

The memory of claim 59 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 173 (canceled)

The memory of claim 172 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 174 (canceled)

The memory of claim 172 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 175 (canceled)

The memory of claim 174 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 176 (canceled)

The memory of claim 59 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 177 (canceled)

The memory of claim 176 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 178 (canceled)

The memory of claim 59 wherein said memory provides at least 256 meg of storage.

Claim 179 (canceled)

The memory of claim 178 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 Meg of storage.

Claim 180 (canceled)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and wherein said power amplifiers are organized into a plurality of groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

Claim 181 (canceled)

The system of claim 180 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein one of said power amplifiers is associated with each of said plurality of array blocks.

Claim 182 (canceled)

The system of claim 181 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 183 (canceled)

The system of claim 180 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate or concurrent operation to achieve predetermined levels of output power.

Claim 184 (canceled)

The system of claim 183 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 185 (canceled)

The system of claim 180 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 186 (canceled)

The system of claim 180 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 187 (canceled)

The system of claim 180 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 188 (canceled)

The system of claim 187 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 189 (canceled)

The system of claim 188 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 190 (canceled)

The system of claim 189 wherein said multiplexers are positioned at every second individual array.

Claim 191 (canceled)

The system of claim 180 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output

buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 192 (canceled)

The system of claim 191 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 193 (canceled)

The system of claim 191 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 194 (canceled)

The system of claim 193 wherein said individual arrays of memory cells include memory cells arranged in rows and column, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 195 (canceled)

The system of claim 180 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 196 (canceled)

The system of claim 195 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to certain of said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 197 (canceled)

The system of claim 180 wherein said memory provides at least 256 meg of storage.

Claim 198 (canceled)

The system of claim 197 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 199 (canceled)

The voltage regulator of claim 60 wherein said plurality of power amplifiers is divided into a plurality of groups for one of independent and concurrent operation among said groups.

Claim 200 (canceled)

The voltage regulator of claim 60 wherein each of said plurality of power amplifiers comprises an amplifier portion and a boost circuit that is operable to increase the slew rate of said amplifier portion in response to said control signals.

Claim 201 (canceled)

The voltage regulator of claim 60 additionally comprising a booster amplifier for supplying additional power to the dynamic random access memory in response to said control signals reflecting a predetermined operating condition.

Claim 202 (canceled)

The voltage regulator of claim 201 wherein said booster amplifier has an output connected through an impedance with an output of said power amplifiers.

Claim 203 (canceled)

The voltage regulator of claim 201 additionally comprising a standby amplifier for supplying power in response to said control signals reflecting periods in which said plurality of power amplifiers and said booster amplifier are not operating.

Claim 204 (canceled)

The voltage regulator of claim 201 wherein said booster amplifier is designed to operate on a bias current less than a bias current required for each of said plurality of power amplifiers.

Claim 205 (canceled)

The voltage regulator of claim 204 wherein said standby amplifier is designed to operate on a bias current less than said bias currents required for each of said plurality of power amplifiers and said booster amplifier.

Claim 206 (canceled)

An amplifier portion of a voltage regulator for a dynamic random access memory, said amplifier portion comprising:

a plurality of power amplifiers divided into a plurality of groups for operation in one of separate or concurrent operation to achieve predetermined levels of power output to the dynamic random access memory.

Claim 207 (canceled)

The amplifier portion of claim 206 additionally comprising a booster amplifier for supplying additional power in response to a predetermined operating condition.

Claim 208 (canceled)

The amplifier portion of claim 207 additionally comprising a standby amplifier for maintaining a nominal level of power output to the dynamic random access memory when said plurality of power amplifiers and said booster amplifier are not operating.

Claim 209 (canceled)

The amplifier portion of claim 206 wherein each of said plurality of power amplifiers has a gain greater than one.

Claim 210 (canceled)

The amplifier portion of claim 206 wherein each of said plurality of power amplifiers comprises an amplifier portion and a boost circuit that is operable to increase the slew rate of said amplifier portion in response to a predetermined operating condition..

Claim 211 (canceled)

A voltage regulator for a dynamic random access memory, comprising:

a circuit for generating a reference voltage from an externally supplied voltage;

an amplifier for amplifying said reference voltage with a gain greater than unity to generate an internal supply voltage available on first and second buses; and

control logic for generating control signals for controlling said amplifier.

Claim 212 (canceled)

The voltage regulator of claim 211 wherein said amplifier comprises a plurality of individual amplifiers arranged substantially in parallel between said circuit for generating a reference voltage and said first bus.

Claim 213 (canceled)

The voltage regulator of claim 212 wherein said first bus carries an array voltage.

Claim 214 (canceled)

The voltage regulator of claim 213 wherein said first bus is connected to said second bus through an impedance.

Claim 215 (canceled)

The voltage regulator of claim 214 wherein said second bus carries a peripheral voltage.

Claim 216 (canceled)

The voltage regulator of claim 211 wherein said amplifier comprises at least one power amplifier, at least one booster amplifier, and at least one standby amplifier, wherein said voltage regulator has reduced operating current requirements by allowing selective operation of the individual amplifiers in one of individual and predetermined combinations.

Claim 217 (canceled)

A method of operating a voltage regulator for a dynamic random access memory, comprising the steps of:

generating a reference voltage from an externally supplied voltage;

amplifying said reference voltage with a gain greater than unity to generate an internal supply voltage available on a bus; and

generating control signals for controlling said step of amplifying

Claim 218 (canceled)

A method of operating an amplifier portion of a voltage regulator for a dynamic random access memory, said method comprising the steps of:

operating at least one power amplifier during periods of memory array operations;

operating, independently of the operating of the at least one power amplifier, at least one booster amplifier during periods of voltage pump operations; and

operating a standby amplifier at a low maintenance current level regardless of the state of operation of the power amplifier and booster amplifier.

Claim 219 (canceled)

The method of claim 218 wherein said step of operating the standby amplifier includes operating the standby amplifier at a current level that is less than that required for operating the at least one power amplifier.

Claim 220 (canceled)

The method of claim 218 wherein said step of operating the at least one power amplifier comprises the step of operating a plurality of power amplifiers in groups to match the power produced to the power required by the memory.

Claim 221 (canceled)

The method of claim 220 wherein said step of operating a plurality of power amplifiers in groups includes operating a plurality of power amplifiers in groups to perform refresh operations at various rates.

Claim 222 (canceled)

The method of claim 218 wherein said steps of operating at least one power amplifier and operating at least one booster amplifier are carried out while maintaining an impedance between the respective outputs of the at least one power amplifier and the at least one booster amplifier to avoid transfer of transients.

Claim 223 (canceled)

A voltage reference circuit responsive to an external voltage for supplying a reference voltage, comprising:

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage; and

a unity gain amplifier responsive to said reference signal for producing the reference voltage.

Claim 224 (canceled)

The voltage reference circuit of claim 223 wherein said active reference circuit comprises a current source providing current to a diode stack having an adjustable impedance for producing said reference signal.

Claim 225 (canceled)

The voltage reference circuit of claim 224 wherein said diode stack includes a plurality of transistors connected in series, with each transistor's gate connected to a common potential, and a plurality of switches each for selectively shunting one of said transistors.

Claim 226 (canceled)

The voltage reference circuit of claim 225 wherein said switches are controlled by fuses, and wherein opening certain of said fuses turns its associated switch on, and wherein opening certain other of said fuses turns its associated switch off.

Claim 227 (canceled)

The voltage reference circuit of claim 226 wherein said plurality of transistors includes a first plurality of field effect transistors and wherein said plurality of switches includes a second plurality of field effect transistors.

Claim 228 (canceled)

The voltage reference circuit of claim 223 additionally comprising a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a predetermined value.

Claim 229 (canceled)

The voltage reference circuit of claim 228 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

Claim 230 (canceled)

The voltage reference circuit of claim 229 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

Claim 231 (canceled)

A voltage reference circuit in combination with a power amplifier, said combination comprising:

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship to the external voltage;

a unity gain amplifier responsive to said reference signal for producing a reference voltage; and

a power amplifier stage for amplifying the reference voltage by a factor greater than unity to provide an output voltage.

Claim 232 (canceled)

The combination of claim 231 additionally comprising a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value.

Claim 233 (canceled)

The combination of claim 232 wherein said circuit for supplying includes a switch for shorting a bus carrying the external voltage with a bus carrying the output voltage.

Claim 234 (canceled)

The combination of claim 232 additionally comprising a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds a second predetermined value.

Claim 235 (canceled)

The combination of claim 234 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

Claim 236 (canceled)

The combination of claim 235 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

Claim 237 (canceled)

The combination of claim 234 wherein said combination supplies an output voltage which increases at a first slope substantially the same as a slope of the external voltage during a powerup range, increases at a second slope substantially less than a slope of the external voltage during an operating range, and increases at a third slope greater than a slope of the external voltage during a burn-in range of the external voltage.

Claim 238 (canceled)

A voltage regulator for a dynamic random access memory for supplying an output voltage in response to an external voltage, and wherein the output voltage has a first characteristic when the external voltage is in a powerup range, has a second characteristic when the external voltage is in an operating range, and has a third characteristic when the external voltage is in a burn-in range, said regulator comprising:

a circuit for supplying the external voltage as the output voltage when the external voltage is below a first predetermined value defining the powerup range;

an active reference circuit for receiving the external voltage and for producing a reference signal having a desired relationship with the external voltage;

a unity gain amplifier responsive to said reference signal for producing a reference voltage when the external voltage is above said first predetermined value;

a power amplifier stage for amplifying the reference voltage by a factor greater than unity to provide the output voltage when said circuit for supplying is not supplying the external voltage as the output voltage; and

a pullup stage for pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds said second predetermined value defining the burn-in range.

Claim 239 (canceled)

The voltage regulator of claim 238 wherein said active reference circuit comprises a current source for presenting a current at a circuit node and a circuit for providing an impedance between said node and a reference potential, said reference signal being available at said node.

Claim 240 (canceled)

The voltage regulator of claim 239 wherein said circuit for providing an impedance includes a circuit for adjusting the impedance to modify said reference signal available at said node.

Claim 241 (canceled)

The voltage regulator of claim 240 wherein said circuit for providing an impedance includes a plurality of transistors connected in series, with each transistor's gate connected to a common potential, and a plurality of switches each for selectively shunting one of said transistors.

Claim 242 (canceled)

The voltage regulator of claim 241 wherein said switches are controlled by fuses, and wherein opening certain of said fuses turns its associated switch on, and wherein opening certain other of said fuses turns its associated switch off.

Claim 243 (canceled)

The voltage regulator of claim 242 wherein said plurality of transistors includes a first plurality of field effect transistors and wherein said plurality of switches includes a second plurality of field effect transistors.

Claim 244 (canceled)

The voltage regulator of claim 238 wherein said pullup stage includes a plurality of diodes connected between the external voltage and the reference voltage.

Claim 245 (canceled)

The voltage regulator of claim 244 wherein the reference voltage is the external voltage less a voltage drop across said plurality of diodes.

Claim 246 (canceled)

The voltage regulator of claim 238 wherein said circuit for supplying includes a switch for shorting a bus carrying the external voltage with a bus carrying the output voltage.

Claim 247 (canceled)

A method of supplying an output voltage in response to an external voltage, and wherein the output voltage has a first characteristic when the external voltage is in a powerup range, has a second characteristic when the external voltage is in an operating range, and has a third characteristic when the external voltage is in a burn-in range, said method comprising the steps of:

supplying the external voltage as the output voltage when the external voltage is below a first predetermined value defining the powerup range;

producing a reference signal having a desired relationship with the external voltage;

amplifying the reference signal with a unity gain amplifier for producing a reference voltage when the external voltage is above said first predetermined value;

amplifying the reference voltage by a factor greater than unity to provide the output voltage when the external voltage is not being supplied as the output voltage; and

pulling up the reference voltage so as to substantially track the external voltage when the external voltage exceeds said second predetermined value defining the burn-in range.

Claim 248 (canceled)

The method of claim 247 wherein said step of producing a reference signal includes the steps of generating a current related to the external voltage, applying the current to a circuit node, and draining the current from the circuit node through an adjustable impedance.

Claim 249 (canceled)

The method of claim 248 additionally comprising the step of adjusting the impedance to modify the reference signal.

Claim 250 (canceled)

The method of claim 249 wherein said step of adjusting the impedance includes the step of opening a fuse.

Claim 251 (canceled)

The memory of claim 61 wherein said logic disables the power amplifier associated with an array block that has had its power distribution switch opened.

Claim 252 (canceled)

The memory of claim 61 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said individual arrays are organized to form said array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 253 (canceled)

The memory of claim 252 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 254 (canceled)

The memory of claim 253 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 255 (canceled)

The memory of claim 254 wherein said multiplexers are positioned at every second individual array.

Claim 256 (canceled)

The memory of claim 61 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O

block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 257 (canceled)

The memory of claim 256 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 258 (canceled)

The memory of claim 256 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 259 (canceled)

The memory of claim 258 wherein said array of memory cells includes memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 260 (canceled)

The memory of claim 61 wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 261 (canceled)

The memory of claim 260 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 262 (canceled)

The memory of claim 61 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 263 (canceled)

The memory of claim 61 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 264 (canceled)

The memory of claim 263 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 265 (canceled)

The memory of claim 61 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

Claim 266 (canceled)

The memory of claim 61 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 267 (canceled)

The memory of claim 61 wherein said memory provides at least 256 meg of storage.

Claim 268 (canceled)

The memory of claim 267 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically

replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 269 (canceled)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells configured in separately controllable array blocks;

a plurality of peripheral devices responsive to external signals for writing data into said array blocks and for reading data out of said array blocks;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage regulator comprised of a plurality of power amplifiers and at least one of said power amplifiers being associated with each of said array blocks;

a plurality of power distribution switches; and

a power distribution bus for delivering said plurality of supply voltages to said array blocks through said plurality of switches and to said plurality of peripheral devices, and wherein said plurality of peripheral devices includes logic for controlling each of said plurality of switches and for controlling the state of each of said power amplifiers.

Claim 270 (canceled)

The system of claim 269 wherein said logic disables the power amplifier associated with an array block that has had its power distribution switch opened.

Claim 271 (canceled)

The system of claim 269 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said individual arrays are organized to form said array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 272 (canceled)

The system of claim 271 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 273 (canceled)

The system of claim 272 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 274 (canceled)

The system of claim 273 wherein said multiplexers are positioned at every second individual array.

Claim 275 (canceled)

The system of claim 269 wherein said plurality of array blocks is organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 276 (canceled)

The system of claim 275 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 277 (canceled)

The system of claim 275 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 278 (canceled)

The system of claim 277 wherein said array of memory cells includes memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 279 (canceled)

The system of claim 269 wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 280 (canceled)

The system of claim 279 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 281 (canceled)

The system of claim 269 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 282 (canceled)

The system of claim 269 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 283 (canceled)

The system of claim 282 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 284 (canceled)

The system of claim 269 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

Claim 285 (canceled)

The system of claim 269 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 286 (canceled)

The system of claim 269 wherein said memory provides at least 256 meg of storage.

Claim 287 (canceled)

The system of claim 286 wherein said plurality of array blocks combine to provide more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 288 (canceled)

The voltage regulator of claim 62 wherein each array block has a capacitance associated therewith, and wherein said control circuitry disables power amplifiers in response to array blocks being disabled so as to maintain a predetermined ratio of the total remaining capacitance to the number of operational power amplifiers.

Claim 289 (canceled)

The voltage regulator of claim 288 wherein said predetermined ratio is approximately 0.25 nanofarads per operational power amplifier.

Claim 290 (canceled)

The voltage regulator of claim 62 wherein said multiple power amplifiers include twelve amplifiers, and wherein eight of said power amplifiers are each associated with one of eight array blocks.

Claim 291 (canceled)

Voltage regulator circuitry for inclusion in a dynamic random access memory, said circuitry comprising:

independent circuits for developing a supply voltage for a plurality of memory array blocks of the dynamic random access memory; and

a control circuit for receiving a signal when one of the memory array blocks is disabled and for producing control signals in response thereto for disabling one of said independent circuits.

Claim 292 (canceled)

The circuitry of claim 291 wherein each array block has a capacitance associated therewith, and wherein said control circuit produces control signals for disabling certain independent circuits in response to array blocks being disabled so as to maintain a predetermined ratio of the total remaining capacitance to the total number of operational independent circuits.

Claim 293 (canceled)

The circuitry of claim 292 wherein said predetermined ratio is approximately 0.25 nanofarads per operational module.

Claim 294 (canceled)

A method of operating an amplifier portion of a voltage regulator for a dynamic random access memory divided into array blocks, said amplifier portion having a number of individual power amplifiers, said method comprising the steps of:

operating at least one power amplifier for each array block during periods when operations are performed by the memory;

determining when an array block has become disabled; and

disabling at least one power amplifier for each disabled array block.

Claim 295 (canceled)

The method of claim 294 wherein each array block has a capacitance associated therewith, and wherein said step of disabling at least one power amplifier includes the step of maintaining a predetermined ratio of the total remaining capacitance to non-disabled power amplifiers.

Claim 296 (canceled)

The method of claim 295 wherein said predetermined ratio is approximately 0.25 nanofarads per non-disabled power amplifier.

Claim 297 (canceled)

A method of operating an amplifier portion of a voltage regulator for a dynamic random access memory divided into eight array blocks, said amplifier portion having a number of individual power amplifiers, said method comprising the steps of:

operating at least one power amplifier for each of the eight array blocks during periods when operations are performed on the memory;

operating the remaining power amplifiers in one of individual and group modes depending on the power requirements of the memory;

determining when an array block has become disabled; and

disabling the power amplifier associated with the disabled array block.

Claim 298 (canceled)

The power supply of claim 63 wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of the plurality of array blocks.

Claim 299 (canceled)

The power supply of claim 298 including circuits for disabling said at least one power amplifier associated with each of the plurality of array blocks when the array block associated therewith is disabled.

Claim 300 (canceled)

The power supply of claim 299 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 301 (canceled)

The power supply of claim 63 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output.

Claim 302 (canceled)

The power supply of claim 301 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 303 (canceled)

The power supply of claim 302 wherein the first type of refresh mode includes a 4k refresh mode and wherein said second type of refresh mode includes an 8k refresh mode.

Claim 304 (canceled)

The power supply of claim 63 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array blocks, said bias generator including an output status monitor.

Claim 305 (canceled)

The power supply of claim 63 wherein said plurality of voltage supplies includes a voltage regulator, a first and a second voltage pumps, and a generator for producing a bias voltage, said memory additionally comprising a powerup sequence circuit for controlling powering up of said voltage regulator, said voltage pumps, and said generator for producing a bias voltage in response to an external voltage.

Claim 306 (canceled)

The memory of claim 64 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 307 (canceled)

The memory of claim 306 wherein the first type of refresh mode includes a 4k refresh mode and wherein the second type of refresh mode includes an 8k refresh mode.

Claim 308 (canceled)

The memory of claim 64 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator including a plurality of power amplifiers, and wherein one of said power amplifiers is associated with each of said plurality of array blocks.

Claim 309 (canceled)

The memory of claim 308 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 310 (canceled)

The memory of claim 309 wherein said plurality of power amplifiers is divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 311 (canceled)

The memory of claim 64 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 312 (canceled)

The memory of claim 311 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 313 (canceled)

The memory of claim 64 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 314 (canceled)

The memory of claim 313 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 315 (canceled)

The memory of claim 314 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 316 (canceled)

The memory of claim 314 wherein said multiplexers are positioned at every other individual array.

Claim 317 (canceled)

The memory of claim 64 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output

buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 318 (canceled)

The memory of claim 317 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 319 (canceled)

The memory of claim 317 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 320 (canceled)

The memory of claim 319 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 321 (canceled)

The memory of claim 64 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 322 (canceled)

The memory of claim 321 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 323 (canceled)

The memory of claim 64 wherein said memory provides at least 256 meg of storage.

Claim 324 (canceled)

The memory of claim 323 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 325 (canceled)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies for generating a plurality of supply voltages, at least one of said voltage supplies being a voltage pump comprised of a plurality of voltage pump circuits and wherein said voltage pump circuits are organized into a plurality of groups operable in one of separate and concurrent operating modes to achieve predetermined levels of output power; and

a power distribution bus for delivering said plurality of supply voltages to said array and said plurality of peripheral devices.

Claim 326 (canceled)

The system of claim 325 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 327 (canceled)

The system of claim 326 wherein the first type of refresh mode includes a 4k refresh mode and wherein the second type of refresh mode includes an 8k refresh mode.

Claim 328 (canceled)

The system of claim 325 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator including a plurality of power amplifiers, and wherein one of said power amplifiers is associated with each of said plurality of array blocks.

Claim 329 (canceled)

The system of claim 328 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 330 (canceled)

The system of claim 329 wherein said plurality of power amplifiers is divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 331 (canceled)

The system of claim 325 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 332 (canceled)

The system of claim 325 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said voltage supplies.

Claim 333 (canceled)

The system of claim 325 wherein said array of memory cells is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 334 (canceled)

The system of claim 333 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 335 (canceled)

The system of claim 334 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 336 (canceled)

The system of claim 334 wherein said multiplexers are positioned at every other individual array.

Claim 337 (canceled)

The system of claim 325 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 338 (canceled)

The system of claim 337 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 339 (canceled)

The system of claim 337 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 340 (canceled)

The system of claim 339 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 341 (canceled)

The system of claim 325 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said power distribution bus includes a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 342 (canceled)

The system of claim 341 additionally comprising a plurality of pads located centrally with respect to said plurality of array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 343 (canceled)

The system of claim 325 wherein said memory provides at least 256 meg of storage.

Claim 344 (canceled)

The system of claim 343 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 345 (canceled)

An output portion of a voltage pump for a dynamic random access memory, comprising:

a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of power output to the dynamic random access memory.

Claim 346 (canceled)

The output portion of claim 345 wherein each of said plurality of voltage pump circuits includes two substantially identical pump portions operating in tandem in response to an externally supplied clock signal.

Claim 347 (canceled)

The output portion of claim 345 wherein said plurality of voltage pump circuits includes twelve pump circuits all of which are operable when the dynamic random access memory is in a first type of refresh mode and wherein only a portion of said twelve pump circuits are operable when the dynamic random access memory is in a second type of fresh mode.

Claim 348 (canceled)

The output portion of claim 347 wherein six of said pump circuits are in a primary group and six of said pump circuits are in a secondary group, and wherein both groups of pump circuits are operable in response to the first type of refresh mode and wherein only said primary group of pump circuits is operable in response to the second type of refresh mode.

Claim 349 (canceled)

The output portion of claim 348 wherein both groups of pump circuits are operable in response to a 4k refresh mode and wherein only said primary group of pump circuits is operable in response to an 8k refresh mode.

Claim 350 (canceled)

The memory of claim 66 wherein said voltage generator is of the type which utilizes a pullup and a pulldown current for regulation purposes, said memory additionally comprising:

a pullup current monitor responsive to the pullup current for generating a first pullup signal and a second pullup signal indicative of whether the change over time of the pullup current is within a second predetermined range; and

a pulldown current monitor responsive to the pulldown current for generating a first pulldown signal and a second pulldown signal indicative of whether the change over time of the pulldown current is within a third predetermined range, and wherein said logic circuit is also responsive to said first and second pullup signals and said first and second pulldown signals.

Claim 351 (canceled)

The memory of claim 66 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 352 (canceled)

The memory of claim 351 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 353 (canceled)

The memory of claim 352 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 354 (canceled)

The memory of claim 353 wherein said multiplexers are positioned at every second individual array.

Claim 355 (canceled)

The memory of claim 66 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of

peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 356 (canceled)

The memory of claim 355 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 357 (canceled)

The memory of claim 355 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 358 (canceled)

The memory of claim 357 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 359 (canceled)

The memory of claim 66 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 360 (canceled)

The memory of claim 359 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 361 (canceled)

The memory of claim 66 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 362 (canceled)

The memory of claim 361 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 363 (canceled)

The memory of claim 361 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 364 (canceled)

The memory of claim 66 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 365 (canceled)

The memory of claim 364 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 366 (canceled)

The memory of claim 66 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 367 (canceled)

The memory of claim 366 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

Claim 368 (canceled)

The memory of claim 66 wherein said memory provides at least 256 meg of storage.

Claim 369 (canceled)

The memory of claim 368 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 370 (canceled)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices responsive to external signals for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices, one of said plurality of voltage supplies including a voltage generator producing an output voltage;

a voltage detection circuit responsive to said output voltage for producing an overvoltage signal and an undervoltage signal indicative of whether the output voltage is within a first predetermined range; and

a logic circuit responsive to said overvoltage and said undervoltage signals for providing an indication of the stability of the voltage generator.

Claim 371 (canceled)

The system of claim 370 wherein said voltage generator is of the type which utilizes a pullup and a pulldown current for regulation purposes, said memory additionally comprising:

a pullup current monitor responsive to the pullup current for generating a first pullup signal and a second pullup signal indicative of whether the change over time of the pullup current is within a second predetermined range; and

a pulldown current monitor responsive to the pulldown current for generating a first pulldown signal and a second pulldown signal indicative of whether the change over time of the pulldown current is within a third predetermined range, and wherein said logic circuit is also responsive to said first and second pullup signals and said first and second pulldown signals.

Claim 372 (canceled)

The system of claim 370 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 373 (canceled)

The system of claim 372 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 374 (canceled)

The system of claim 373 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 375 (canceled)

The system of claim 374 wherein said multiplexers are positioned at every second individual array.

Claim 376 (canceled)

The system of claim 370 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 377 (canceled)

The system of claim 376 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 378 (canceled)

The system of claim 376 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 379 (canceled)

The system of claim 378 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 380 (canceled)

The system of claim 370 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 381 (canceled)

The system of claim 380 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage

from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 382 (canceled)

The system of claim 370 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 383 (canceled)

The system of claim 382 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 384 (canceled)

The system of claim 382 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 385 (canceled)

The system of claim 370 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 386 (canceled)

The system of claim 385 wherein said plurality of voltage pump circuits is divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 387 (canceled)

The system of claim 370 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 388 (canceled)

The system of claim 387 additionally comprising a powerup sequence circuit for controlling the powering up of certain of said plurality of voltage supplies.

Claim 389 (canceled)

The system of claim 370 wherein said memory provides at least 256 meg of storage.

Claim 390 (canceled)

The system of claim 389 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 391 (canceled)

A stability sensor for a voltage generator generating an output voltage, comprising:

a voltage detection circuit responsive to the output voltage for producing an overvoltage signal and an undervoltage signal indicative of whether the output voltage is within a first predetermined range; and

a logic circuit responsive to said overvoltage and said undervoltage signals for providing an indication of the stability of the voltage generator.

Claim 392 (canceled)

The stability sensor of claim 391 wherein said voltage detection circuit includes:

a first transistor responsive to the output voltage for producing said overvoltage signal indicative of whether the output voltage is greater than an upper limit of said first predetermined range; and

a second transistor responsive to the output voltage for producing said undervoltage signal indicative of whether the output voltage is less than a lower limit of said first predetermined range.

Claim 393 (canceled)

The stability sensor of claim 391 wherein said voltage generator is of the type which utilizes a pullup and a pulldown current for regulation purposes, said sensor further comprising:

a pullup current monitor responsive to the pullup current for generating a first pullup signal and a second pullup signal indicative of whether the change over time of the pullup current is within a second predetermined range; and

a pulldown current monitor responsive to the pulldown current for generating a first pulldown signal and a second pulldown signal indicative of whether the change over time of the pulldown current is within a third predetermined range, and wherein said logic circuit is also responsive to said first and second pullup signals and said first and second pulldown signals.

Claim 394 (canceled)

The stability sensor of claim 393 wherein said pullup current monitor includes:

a source circuit for sourcing current, each source current being indicative of the present pullup current;

a sink circuit for sinking current;

an RC time constant circuit connected between said source circuit and said sink circuit such that each sink current is indicative of a previous pullup current;

a positive differential current circuit responsive to the source current and the sink current for generating said first pullup signal indicative of whether the present pullup current is greater than the previous pullup current; and

a negative differential current circuit responsive to the source current and the sink current for generating said second pullup signal indicative of whether the present pullup current is less than the previous pullup current.

Claim 395 (canceled)

The stability sensor of claim 394 wherein said sink circuit includes a transistor controlled by said RC time constant circuit.

Claim 396 (canceled)

The stability sensor of claim 394 wherein said RC time constant circuit includes a resistor in combination with a capacitor, and wherein a charge stored by said capacitor is responsive to the difference between the source current and the sink current.

Claim 397 (canceled)

The stability sensor of claim 394 wherein said positive differential circuit includes a resistor connected to produce a voltage indicative of the difference between the source current and the sink current and an inverter responsive to said voltage.

Claim 398 (canceled)

The stability sensor of claim 394 wherein said negative differential circuit includes a resistor connected to produce a voltage indicative of the difference between the source current and the sink current and a pair of series connected inverters responsive to said voltage.

Claim 399 (canceled)

The stability sensor of claim 393 wherein said pulldown current monitor includes:

a sink circuit for sinking current, each sink current being indicative of the present pulldown current;

a source circuit for sourcing current;

an RC time constant circuit connected between said sink circuit and said source circuit such that each source current is indicative of a previous pulldown current;

a positive differential current circuit responsive to the sink current and the source current for generating said first pulldown signal indicative of whether the present pulldown current is greater than the previous pulldown current; and

a negative differential current circuit responsive to the sink current and the source current for generating said second pulldown signal indicative of whether the present pulldown current is less than the previous pulldown current.

Claim 400 (canceled)

The stability sensor of claim 398 wherein said source circuit includes a transistor controlled by said RC time constant circuit.

Claim 401 (canceled)

The stability sensor of claim 399 wherein said RC time constant circuit includes a resistor in combination with a capacitor, and wherein a charge stored by said capacitor is responsive to the difference between the sink current and the source current.

Claim 402 (canceled)

The stability sensor of claim 399 wherein said positive differential circuit includes a resistor connected to produce a voltage indicative of the difference between the sink current and the source current and an inverter responsive to said voltage.

Claim 403 (canceled)

The stability sensor of claim 399 wherein said negative differential circuit includes a resistor connected to produce a voltage indicative of the difference between the sink current and the source current and a pair of series connected inverters responsive to said voltage.

Claim 404 (canceled)

The memory of claim 68 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays in said array blocks and a plurality of row decoders positioned between adjacent columns of individual arrays in said array blocks.

Claim 405 (canceled)

The memory of claim 404 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 406 (canceled)

The memory of claim 405 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with

said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 407 (canceled)

The memory of claim 406 wherein said multiplexers are positioned at every second individual array.

Claim 408 (canceled)

The memory of claim 68 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 409 (canceled)

The memory of claim 408 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 410 (canceled)

The memory of claim 408 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 411 (canceled)

The memory of claim 410 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 412 (canceled)

The memory of claim 68 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 413 (canceled)

The memory of claim 412 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 414 (canceled)

The memory of claim 68 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 415 (canceled)

The memory of claim 414 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 416 (canceled)

The memory of claim 414 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 417 (canceled)

The memory of claim 68 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 418 (canceled)

The memory of claim 417 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 419 (canceled)

The memory of claim 68 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 420 (canceled)

The memory of claim 68 wherein said powerup sequence circuit controls the powering up of certain of said plurality of voltage supplies in response to an externally supplied voltage.

Claim 421 (canceled)

The memory of claim 68 wherein said memory provides at least 256 meg of storage.

Claim 422 (canceled)

The memory of claim 421 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 423 (canceled)

A system, comprising:

a control unit for performing a series of instructions; and

a dynamic random access memory responsive to said control unit, said memory comprising:

an array of memory cells;

a plurality of peripheral devices for writing data into said memory cells and for reading data out of said memory cells;

a plurality of voltage supplies responsive to an external voltage for generating a plurality of supply voltages for use by said array and said plurality of peripheral devices; and

a powerup sequence circuit for controlling the powering up of certain of the plurality of voltage supplies in response to the condition of previously powered up voltage supplies.

Claim 424 (canceled)

The system of claim 423 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

Claim 425 (canceled)

The system of claim 424 wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

Claim 426 (canceled)

The system of claim 425 wherein said array blocks include datalines running between adjacent columns of individual arrays and through said row decoders to form intersections with said I/O lines, said plurality of peripheral devices including a plurality of multiplexers positioned at certain of said intersections of I/O lines and datalines for transferring signals on said I/O lines to said datalines.

Claim 427 (canceled)

The system of claim 426 wherein said multiplexers are positioned at every second individual array.

Claim 428 (canceled)

The system of claim 423 wherein said array of memory cells includes a plurality of individual arrays organized into a plurality of array quadrants, and wherein said plurality of

peripheral devices includes an array I/O block for servicing each of said array quadrants, a plurality of data read multiplexers responsive to said array I/O blocks, a plurality of data output buffers responsive to said plurality of data read multiplexers, and a plurality of data pad drivers responsive to said plurality of data output buffers.

Claim 429 (canceled)

The system of claim 428 wherein said plurality of peripheral devices includes a plurality of data in buffers responsive to externally supplied data and a plurality of data write multiplexers responsive to said plurality of data in buffers, and wherein said array I/O blocks are responsive to said plurality of data write multiplexers.

Claim 430 (canceled)

The system of claim 428 additionally comprising a data test path circuit interposed between said array I/O blocks and said plurality of data read multiplexers.

Claim 431 (canceled)

The system of claim 430 wherein said individual arrays of memory cells include memory cells arranged in rows and columns, said memory additionally comprising logic for cycling through sets of rows of cells in response to an all row high test request.

Claim 432 (canceled)

The system of claim 423 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.

Claim 433 (canceled)

The system of claim 432 additionally comprising a plurality of pads located centrally with respect to said array blocks, and wherein said power distribution bus includes a third plurality of conductors running parallel to said plurality of pads for receiving an external voltage from said plurality of pads and for distributing the external voltage to said plurality of voltage supplies.

Claim 434 (canceled)

The system of claim 423 wherein said array of memory cells is organized into a plurality of array blocks, and wherein said plurality of voltage supplies includes a voltage regulator comprised of a plurality of power amplifiers, and wherein at least one power amplifier is associated with each of said plurality of array blocks.

Claim 435 (canceled)

The system of claim 434 additionally comprising circuits for disabling said at least one power amplifier when its associated array block is disabled.

Claim 436 (canceled)

The system of claim 434 wherein said plurality of power amplifiers is divided into a plurality of groups for one of separate and concurrent operation to achieve a predetermined level of output power.

Claim 437 (canceled)

The system of claim 423 wherein said plurality of voltage supplies includes a voltage pump including a plurality of voltage pump circuits divided into a plurality of groups for operation in one of separate and concurrent operation to achieve predetermined levels of output power.

Claim 438 (canceled)

The system of claim 437 wherein said plurality of voltage pump circuits are divided into a primary group and a secondary group, and wherein both said primary and said secondary groups are operable in response to a first type of refresh mode and wherein only said primary group is operable in response to a second type of refresh mode.

Claim 439 (canceled)

The system of claim 423 wherein said plurality of voltage supplies includes a bias generator for supplying a bias voltage to said array, said bias generator including an output status monitor.

Claim 440 (canceled)

The system of claim 423 wherein said powerup sequence circuit controls the powering up of certain of said plurality of voltage supplies in response to an externally supplied voltage.

Claim 441 (canceled)

The system of claim 423 wherein said memory provides at least 256 meg of storage.

Claim 442 (canceled)

The system of claim 441 wherein said array provides more than 256 meg of storage, said memory additionally comprising repair logic to logically replace defective memory cells with operable memory cells such that said memory provides said 256 meg of storage.

Claim 443 (canceled)

A device responsive to first and second external signals for controlling a power up of a first voltage supply, comprising:

a first circuit responsive to the first external signal for producing a first output signal indicative of whether the first external signal satisfies a predetermined condition; and

a second circuit responsive to the first output signal and the second external signal for producing a first enable signal to enable the first voltage supply.

Claim 444 (currently amended)

A device responsive to first and second external signals for controlling a power up of a first voltage supply, comprising:

a first circuit responsive to the first external signal for producing a first output signal indicative of whether the first external signal is ~~The device of claim 443, wherein said first output signal is indicative of the first external signal being~~ greater than a first predetermined voltage.; and

a second circuit responsive to the first output signal and the second external signal for producing a first enable signal to enable the first voltage supply.

Claim 445 (previously presented)

The device of claim 444, wherein said first predetermined voltage is approximately two volts.

Claim 446 (previously presented)

The device of claim 444, wherein said first circuit includes:

a first voltage detector responsive to the first external signal for producing a first signal indicative of the first external signal being greater than said first predetermined voltage;

a second voltage detector responsive to the first external signal for producing a second signal indicative of the first external signal being greater than said first predetermined voltage; and

a logic circuit responsive to said first and second signals for producing said first output signal.

Claim 447 (previously presented)

The device of claim 446, wherein said first voltage detector includes:

a voltage limiting circuit responsive to the first external signal for producing a threshold signal; and

a signal generating circuit responsive to the first external signal and said threshold signal for producing said first signal.

Claim 448 (canceled)

The device of claim 447, wherein said second predetermined voltage is approximately 0.7 volts.

Claim 449 (previously presented)

The device of claim 447, wherein said voltage limiting circuit includes:

a resistor having a first end and a second end, said first end in communication with the first external signal;

a plurality of series-connected, p-channel transistors each having a gate terminal in communication with a reference potential, with one of said transistors having a source terminal in communication with said second end of said resistor for producing said threshold signal, and

another of said transistors having a drain terminal in communication with said reference potential, said transistors being capable of being shorted across their source and drain terminals to change the value of said threshold signal.

Claim 450 (previously presented)

The device of claim 449, wherein said signal generating circuit includes:

a resistor having a first end and a second end, said first end in communication with a reference potential; and

a p-channel transistor having a source terminal in communication with the first external signal, a gate terminal in communication with the threshold signal, and a drain terminal in communication with said second end of said resistor for producing said first signal.

Claim 451 (previously presented)

The device of claim 446, wherein said second voltage detector includes:

a voltage limiting circuit responsive to the first external signal for producing a threshold signal; and

a signal generating circuit responsive to the first external signal and said threshold signal for producing said second signal.

Claim 452 (canceled)

The device of claim 451, wherein said second predetermined voltage is approximately 0.7 volts.

Claim 453 (previously presented)

The device of claim 451, wherein said voltage limiting circuit includes:

a resistor having a first end and a second end, said first end in communication with a reference potential;

a plurality of series-connected, n-channel transistors each having a gate terminal in communication with the first external signal, with one of said transistors having a drain terminal in communication with the first external signal, and another of said transistors having a source terminal in communication with said second end of said resistor for producing the threshold signal, said transistors being capable of being shorted across their source and drain terminals to change the value of said threshold signal.

Claim 454 (previously presented)

The device of claim 453, wherein said signal generating circuit includes:

a resistor having a first end and a second end, said first end in communication with the first external signal; and

an n-channel transistor having a source terminal in communication with the reference potential, a gate terminal in communication with said threshold signal, and a drain terminal in communication with said second end of said resistor for producing said second signal.

Claim 455 (previously presented)

The device of claim 446, wherein said logic circuit includes:

first and second series connected inverters for receiving said first signal;

a third inverter for receiving said second signal;

a NAND gate responsive to said series connected first and second inverters and said third invertor; and

a fourth inverter responsive to said NAND gate for producing said first output signal.

Claim 456 (currently amended)

The device of claim ~~443~~ 444, additionally comprising a reset circuit interposed between said first and second circuits for receiving said first output signal from said first circuit and for terminating said first output signal when predetermined stability requirements are not met.

Claim 457 (previously presented)

The device of claim 456, wherein said predetermined stability requirements include said first output signal remaining within a predetermined range for approximately one hundred nanoseconds.

Claim 458 (previously presented)

The device of claim 456 wherein said reset circuit includes:

a plurality of series-connected buffer gates with a first one of said buffer gates responsive to said first output signal; and

a logic circuit responsive to said first output signal and a last one of said series-connected buffer gates.

Claim 459 (previously presented)

The device of claim 458, wherein said reset circuit includes:

a NAND gate having a first input terminal in communication with said first output signal, a second input terminal in communication with said last one of said series-connected buffer gates, and an output terminal; and

an inverter having an input terminal in communication with said output terminal of said NAND gate, and an output terminal at which said first output signal is available.

Claim 460 (previously presented)

The device of claim 458 wherein said reset circuit further includes a reset logic gate responsive to said first output signal for producing a reset signal for resetting said buffer gates to a predetermined state.

Claim 461 (currently amended)

The device of claim ~~443~~ 444, wherein said second circuit includes:

a logic circuit responsive to said first output signal and the second external signal for producing an output signal; and

a latch responsive to said output signal of said logic circuit for producing said first enable signal.

Claim 462 (previously presented)

The device of claim 461, wherein said logic circuit includes a NAND gate having a first input terminal in communication with said first output signal, a second input terminal in communication with the second external signal, and an output terminal for producing said output signal of said logic circuit.

Claim 463 (currently amended)

The device of claim ~~443~~ 444, wherein said device is responsive to a third external signal for controlling the power up sequence of a second voltage supply, said device comprising:

a third circuit responsive to said first output signal, the second external signal, and the third external signal for producing a second enable signal to enable the second voltage supply.

Claim 464 (previously presented)

The device of claim 463, wherein said third circuit includes:

a logic circuit responsive to said first output signal, the second external signal, and the third external signal for producing an output signal; and

a latch responsive to said output signal of said logic circuit for producing said second enable signal.

Claim 465 (previously presented)

The device of claim 464, wherein said logic circuit includes:

a NAND gate having a first input terminal in communication with said first output signal, a second input terminal in communication with the second external signal, a third input terminal in communication with the third external signal, and an output terminal for producing said output signal of said logic circuit.

Claim 466 (previously presented)

A device for controlling the powering up of a first voltage supply, comprising:

a first voltage detector constructed of substantially identical p-channel and n-channel devices for producing a first output signal indicative of a first external signal being greater than a predetermined voltage substantially independently of process variations;

a reset circuit responsive to said first voltage detector for outputting said first output signal when said first external signal is stable;

a logic circuit responsive to said reset circuit and a second external signal; and

a latch responsive to said logic circuit for producing a first enable signal for controlling the powering up of a first voltage supply.

Claim 467 (previously presented)

The device of claim 466 wherein said reset circuit comprises:

a plurality of series-connected buffers with a first one of said buffers responsive to said first output signal; and

a logic circuit responsive to said first output signal and a last one of said series-connected buffers.

Claim 468 (previously presented)

The device of claim 467 wherein said reset circuit is constructed such that the first external signal must remain within a predetermined range for approximately one hundred nanoseconds for said logic circuit to output said first output signal.

Claim 469 (previously presented)

A device for controlling the powering up of a first voltage supply, comprising:

a first voltage detector comprised of p-channel devices for producing a first signal indicative of a first external signal being greater than a first predetermined voltage;

a second voltage detector comprised of n-channel devices for producing a second signal indicative of the first external signal being greater than said first predetermined voltage;

a logic circuit responsive to said first and second signals for producing a first output signal;

a reset circuit responsive to said first output signal;

a logic circuit responsive to said reset circuit and a second external signal; and

a latch responsive to said logic circuit for producing a first enable signal for controlling the powering up of a first voltage supply.

Claim 470 (previously presented)

The device of claim 469 wherein said reset circuit comprises:

a plurality of series-connected buffers with a first one of said buffers responsive to said first output signal; and

a logic circuit responsive to said first output signal and a last one of said series-connected buffers.

Claim 471 (previously presented)

The device of claim 470 wherein said reset circuit is constructed such that the first external signal must remain within a predetermined range for approximately one hundred nanoseconds for said logic circuit to output said first output signal.

Claim 472 (previously presented)

A device for an integrated circuit having a voltage supply responsive to a voltage external to the integrated circuit and generating a feedback signal, said device comprising:

a first circuit portion responsive to the external voltage for producing a first output signal indicative of whether the external voltage is above a predetermined value; and

a second circuit portion responsive to said first output signal and the feedback signal for producing a first enable signal to enable the voltage supply.

Claim 473 (previously presented)

The device of claim 472, wherein said first circuit portion includes:

a first voltage detector constructed of p-type components and responsive to the external voltage for producing a first signal indicative of the external voltage being greater than said predetermined value;

a second voltage detector constructed of n-type components and responsive to the external voltage for producing a second signal indicative of the external voltage being greater than said predetermined value; and

a logic circuit responsive to said first and second signals for producing said first output signal.

Claim 474 (previously presented)

The device of claim 472, wherein said second circuit portion includes:

a logic circuit responsive to said first output signal and the feedback signal for producing an output signal; and

a latch responsive to said output signal of said logic circuit for producing said first enable signal.

Claim 475 (previously presented)

The device of claim 472, additionally comprising a reset circuit interposed between said first and second circuit portions for receiving said first output signal from said first circuit portion and for terminating said first output signal when predetermined stability requirements are not meet.